FIG. 1

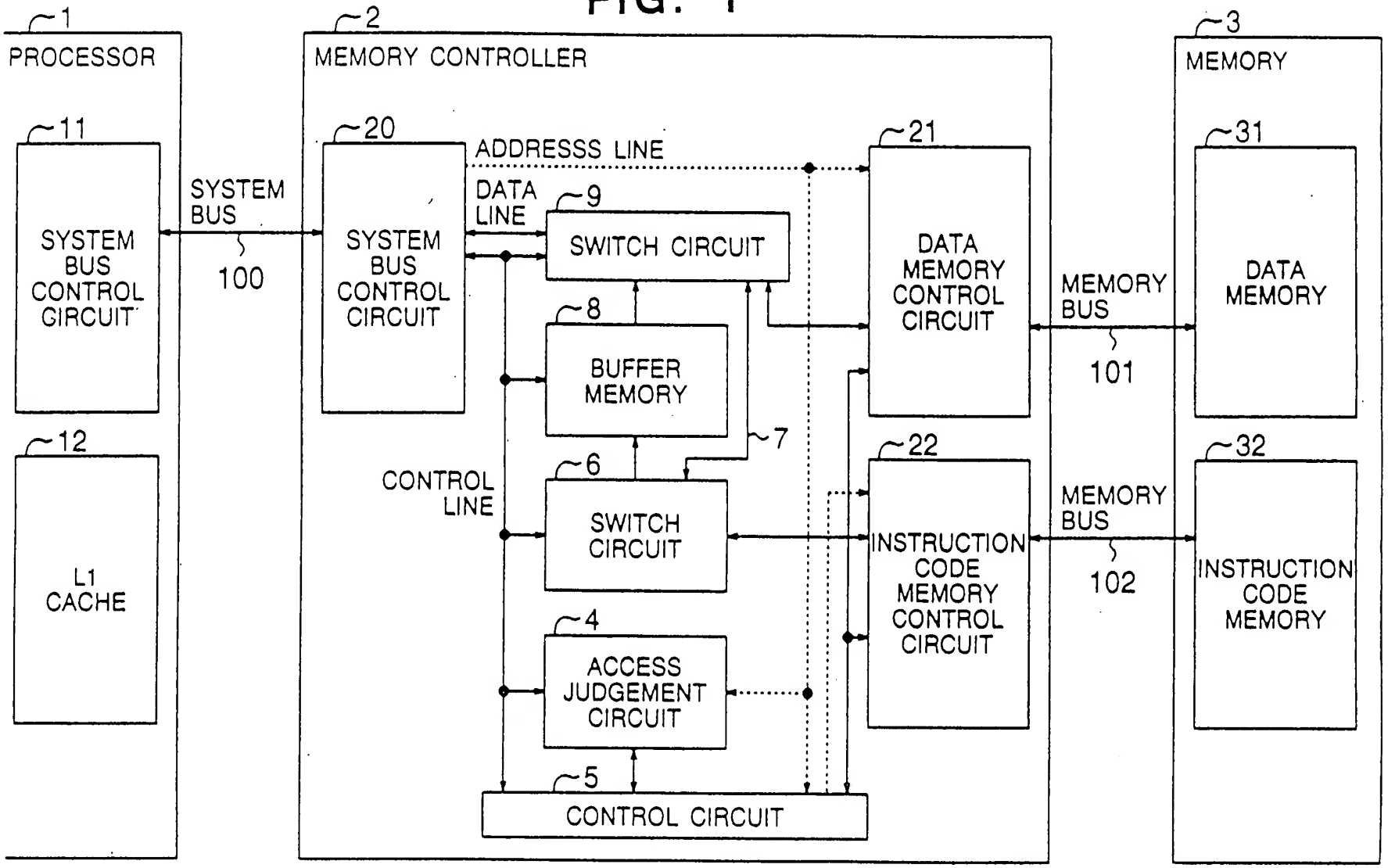

FIG. 2

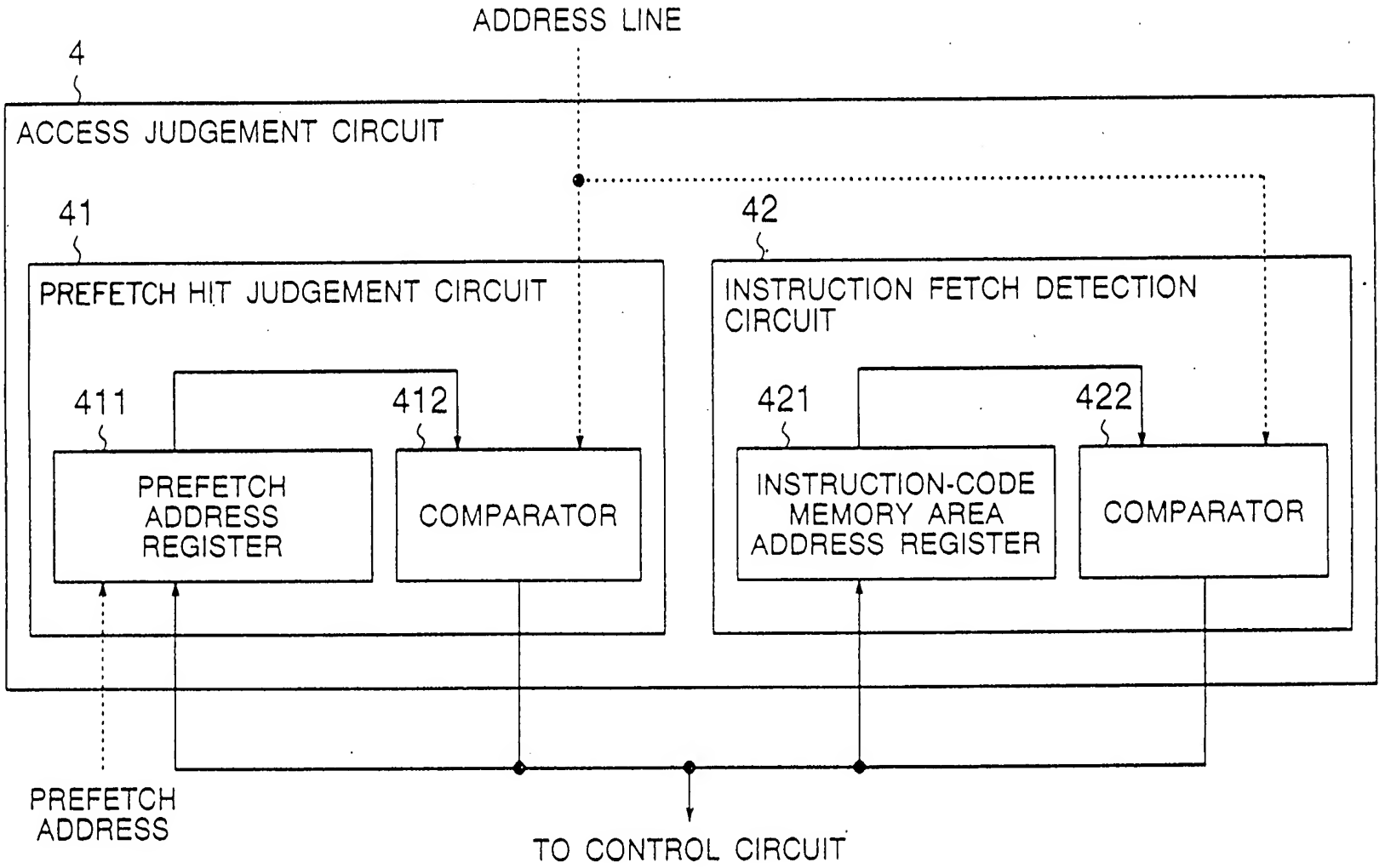
ADDRESS LINE
4
ACCESS JUDGEMENT CIRCUIT
41
PREFETCH HIT JUDGEMENT CIRCUIT
411
412
PREFETCH ADDRESS REGISTER
COMPARATOR
42
INSTRUCTION FETCH DETECTION CIRCUIT
421
422
INSTRUCTION-CODE MEMORY AREA ADDRESS REGISTER
COMPARATOR
PREFETCH ADDRESS
TO CONTROL CIRCUIT

FIG. 3

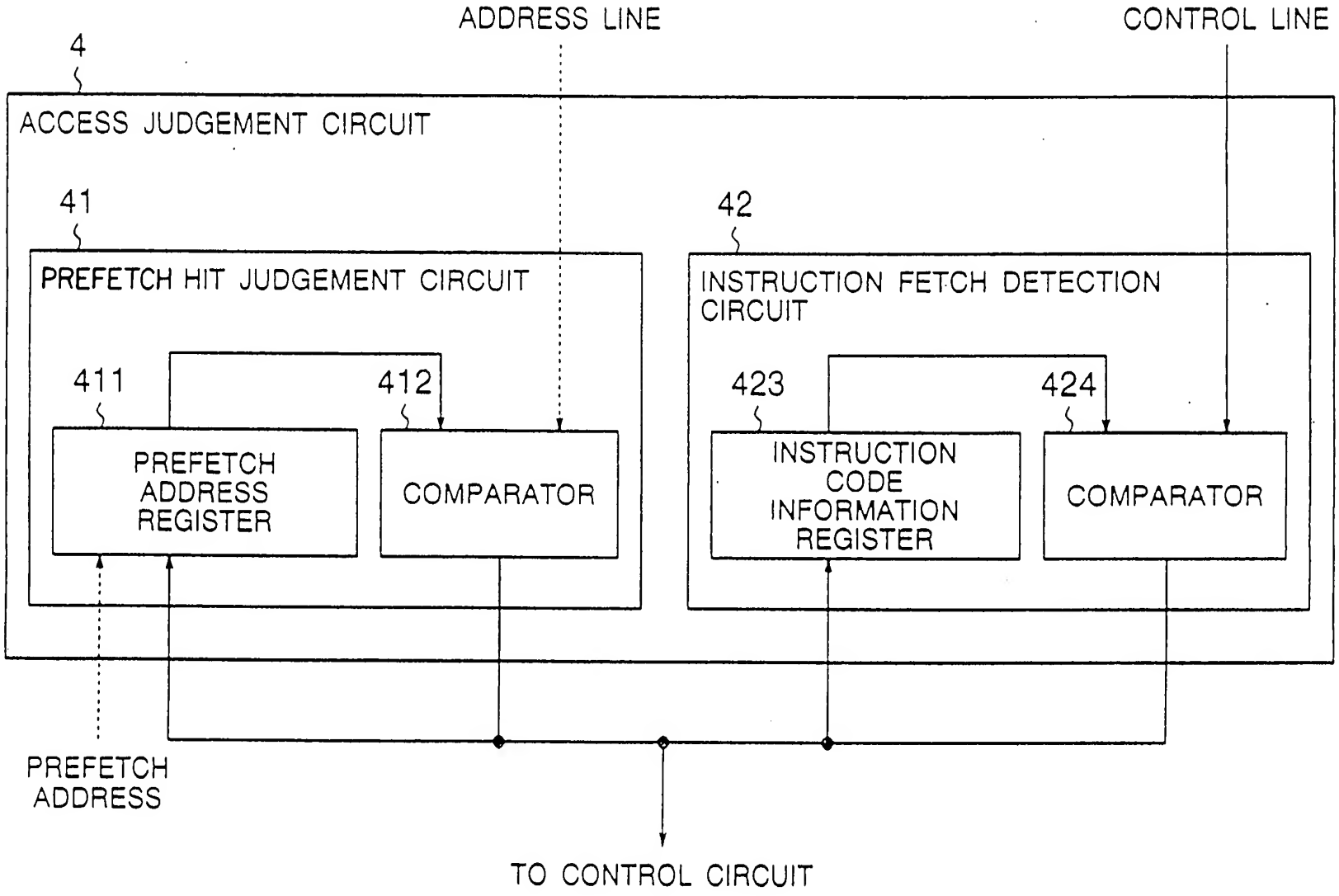

FIG. 4

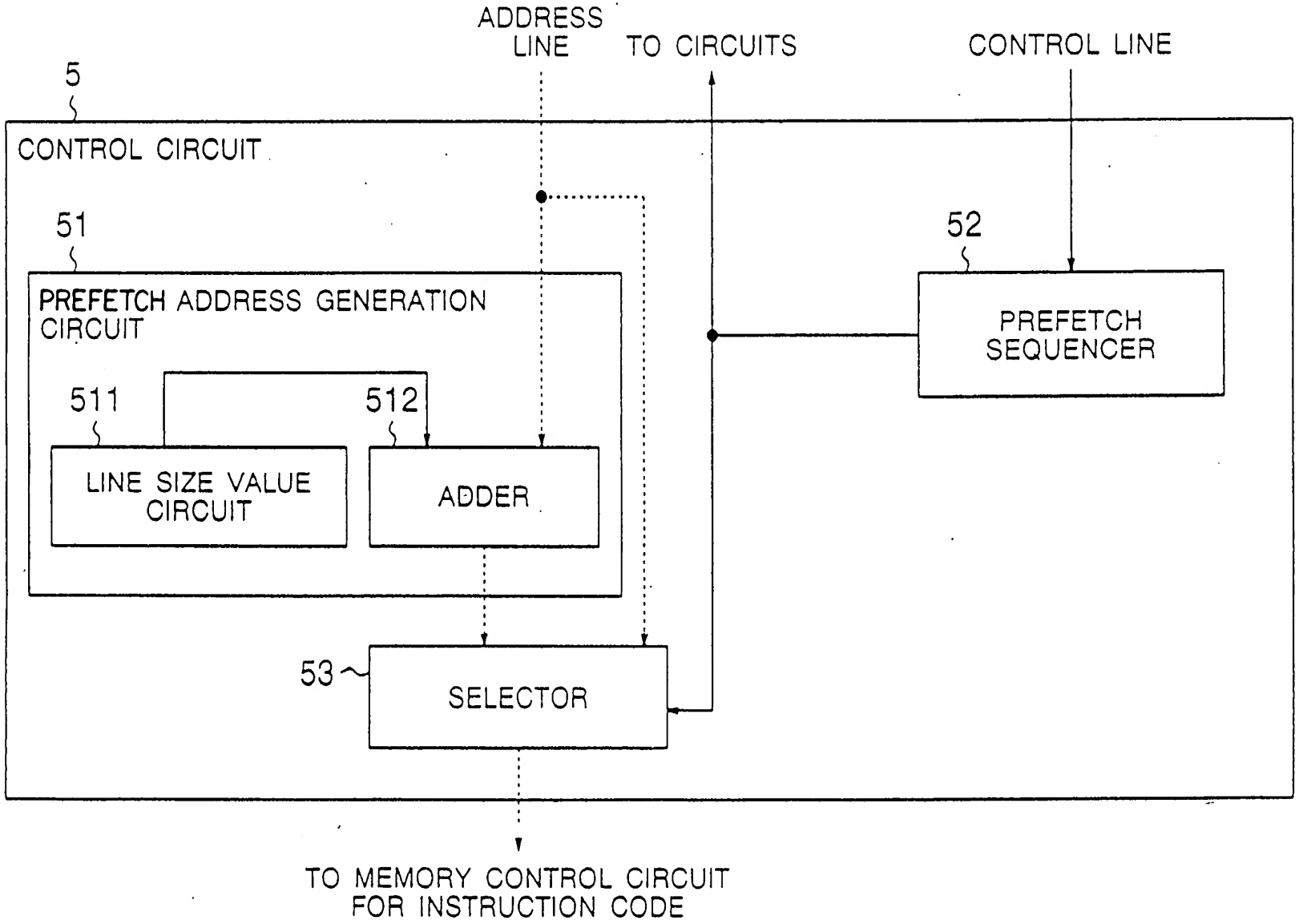
ADDRESS LINE
TO CIRCUITS
CONTROL LINE
5
CONTROL CIRCUIT
51
PREFETCH ADDRESS GENERATION CIRCUIT
511
LINE SIZE VALUE CIRCUIT
512
ADDER
52
PREFETCH SEQUENCER
53
SELECTOR
TO MEMORY CONTROL CIRCUIT FOR INSTRUCTION CODE

FIG. 5

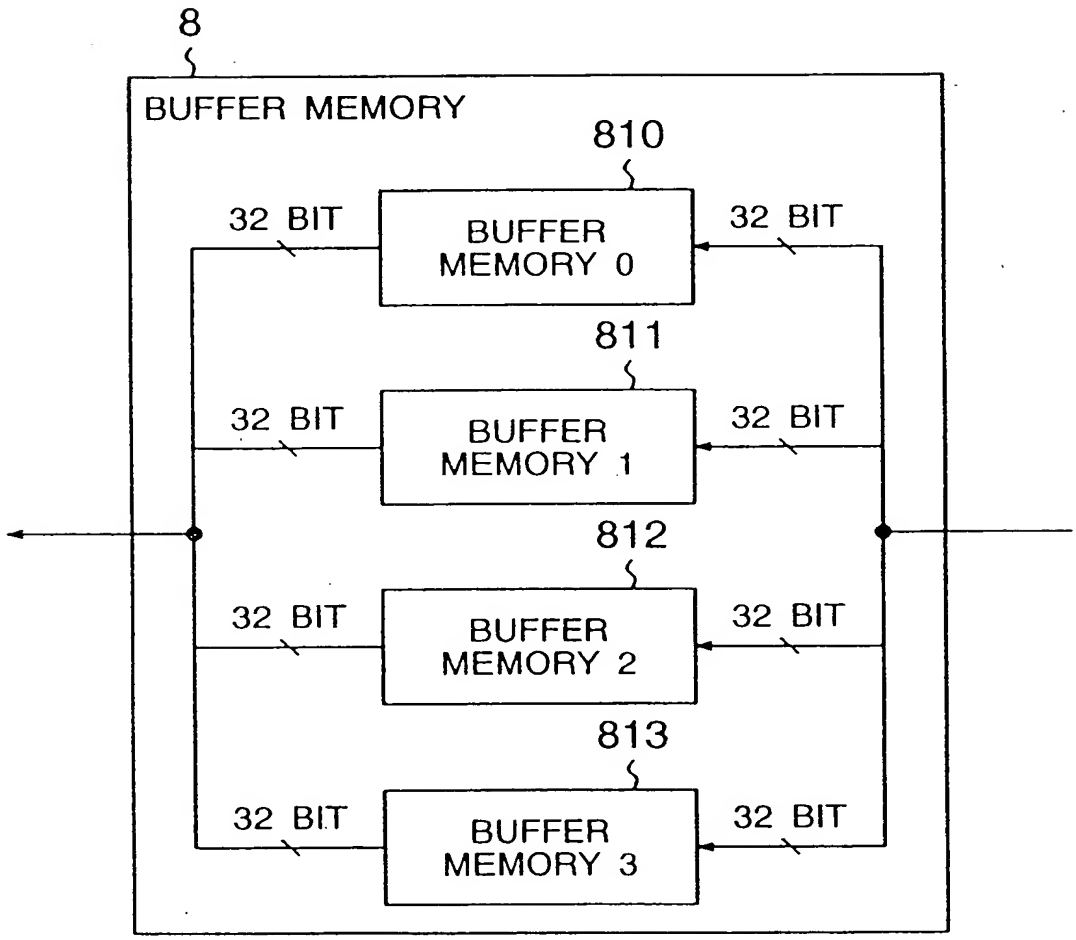
8
BUFFER MEMORY
810
32 BIT
BUFFER MEMORY 0
32 BIT
811
32 BIT
BUFFER MEMORY 1
32 BIT
812
32 BIT
BUFFER MEMORY 2
32 BIT
813
32 BIT
BUFFER MEMORY 3
32 BIT

FIG. 6

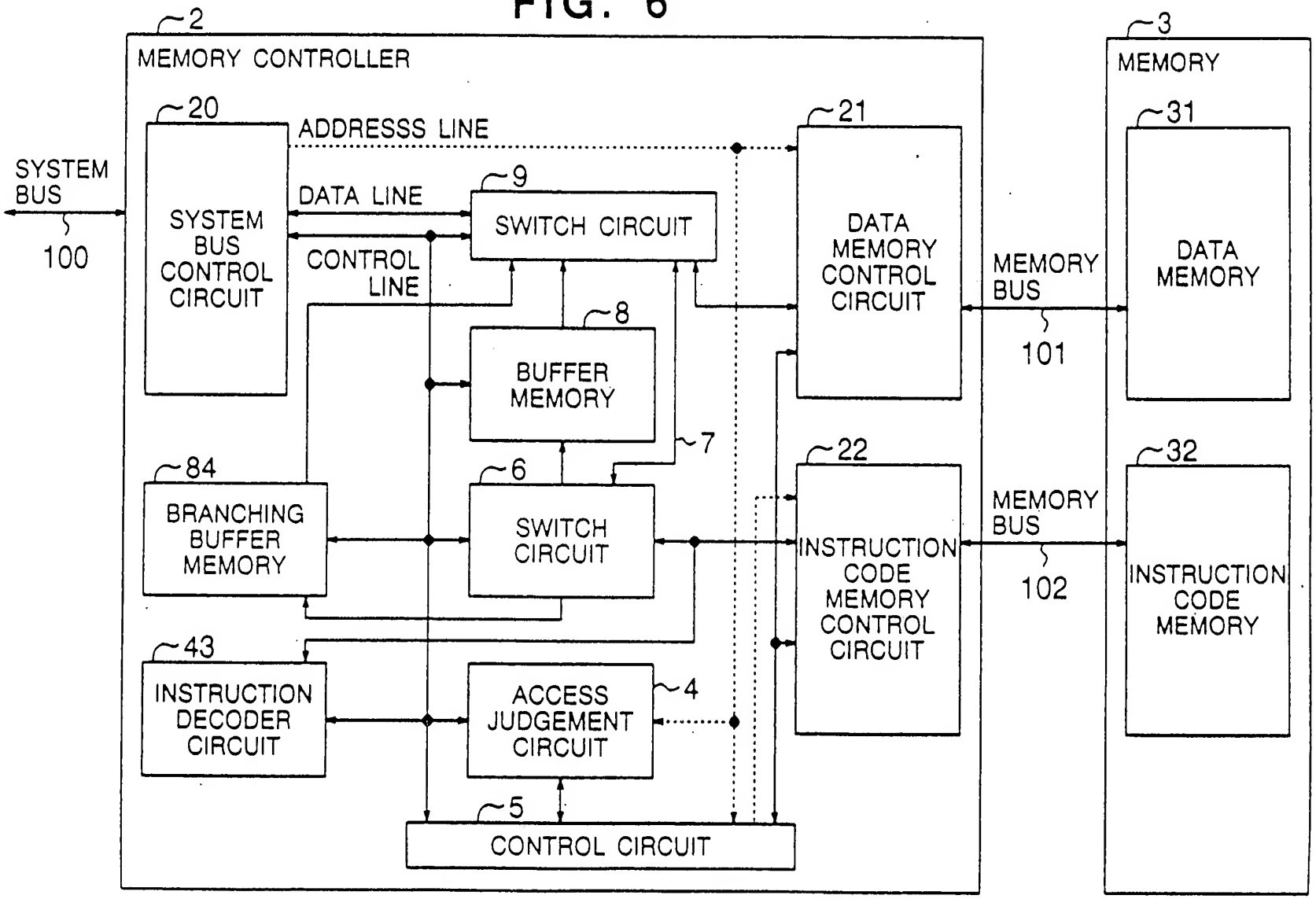
2
MEMORY CONTROLLER
20
ADDRESSS LINE
SYSTEM BUS
100
SYSTEM BUS CONTROL CIRCUIT
DATA LINE
9
SWITCH CIRCUIT
CONTROL LINE
8
BUFFER MEMORY
7
84
BRANCHING BUFFER MEMORY
6
SWITCH CIRCUIT
43
INSTRUCTION DECODER CIRCUIT
ACCESS JUDGEMENT CIRCUIT
4
5
CONTROL CIRCUIT
21
DATA MEMORY CONTROL CIRCUIT
22
INSTRUCTION CODE MEMORY CONTROL CIRCUIT
MEMORY BUS
101
MEMORY BUS
102
3
MEMORY
31
DATA MEMORY
32
INSTRUCTION CODE MEMORY

FIG. 7

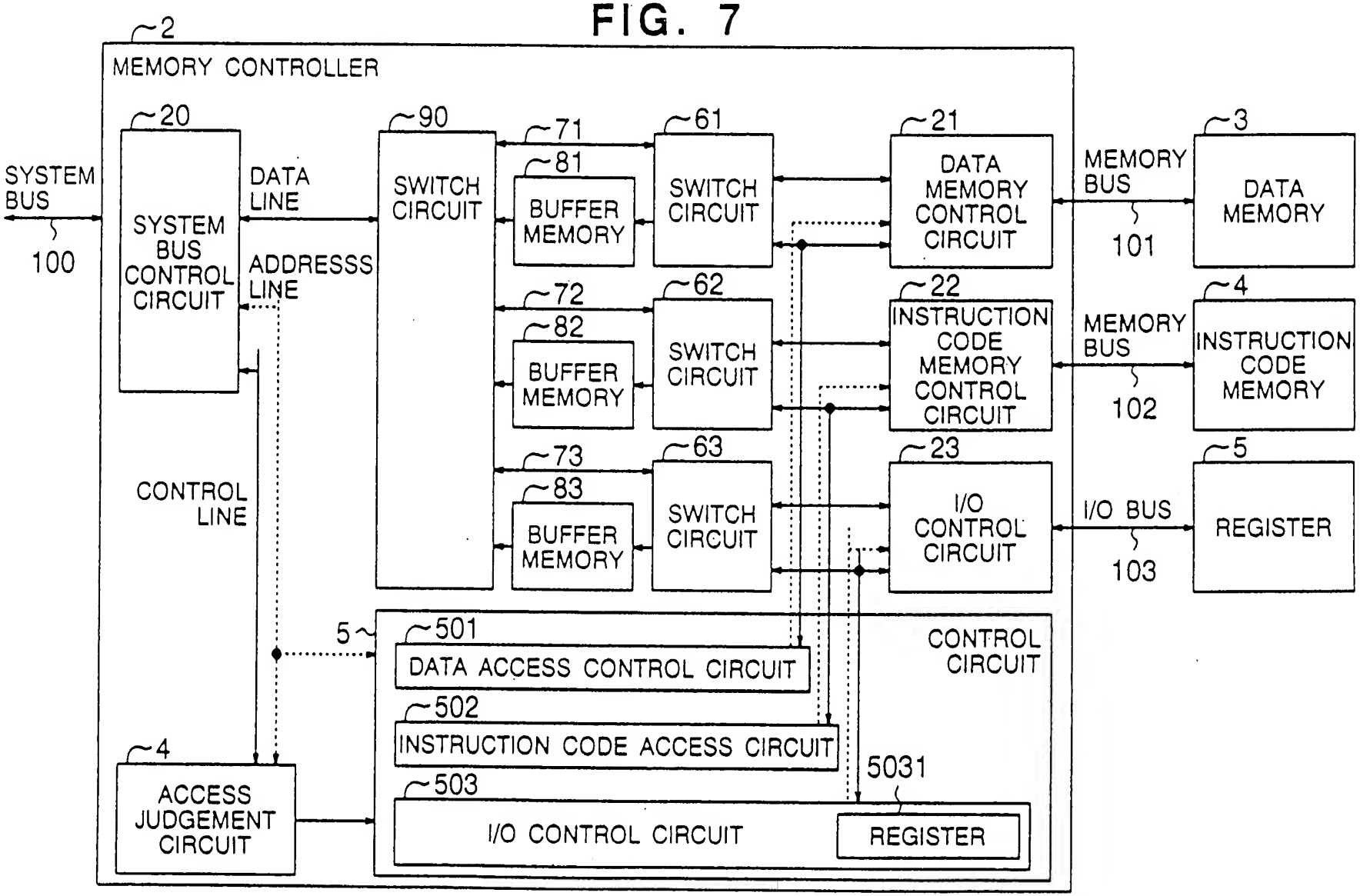
2
MEMORY CONTROLLER
20
SYSTEM BUS
100
SYSTEM BUS CONTROL CIRCUIT
DATA LINE
ADDRESSS LINE
CONTROL LINE
90
SWITCH CIRCUIT
71
81
BUFFER MEMORY
61
SWITCH CIRCUIT
72
82
BUFFER MEMORY
62
SWITCH CIRCUIT
73
83
BUFFER MEMORY
63
SWITCH CIRCUIT
21
DATA MEMORY CONTROL CIRCUIT
22
INSTRUCTION CODE MEMORY CONTROL CIRCUIT
23
I/O CONTROL CIRCUIT
MEMORY BUS
101
MEMORY BUS
102
I/O BUS
103
3
DATA MEMORY
4
INSTRUCTION CODE MEMORY
5
REGISTER
5
501
DATA ACCESS CONTROL CIRCUIT
502
INSTRUCTION CODE ACCESS CIRCUIT
503
I/O CONTROL CIRCUIT
5031
REGISTER
CONTROL CIRCUIT
4
ACCESS JUDGEMENT CIRCUIT

FIG. 8

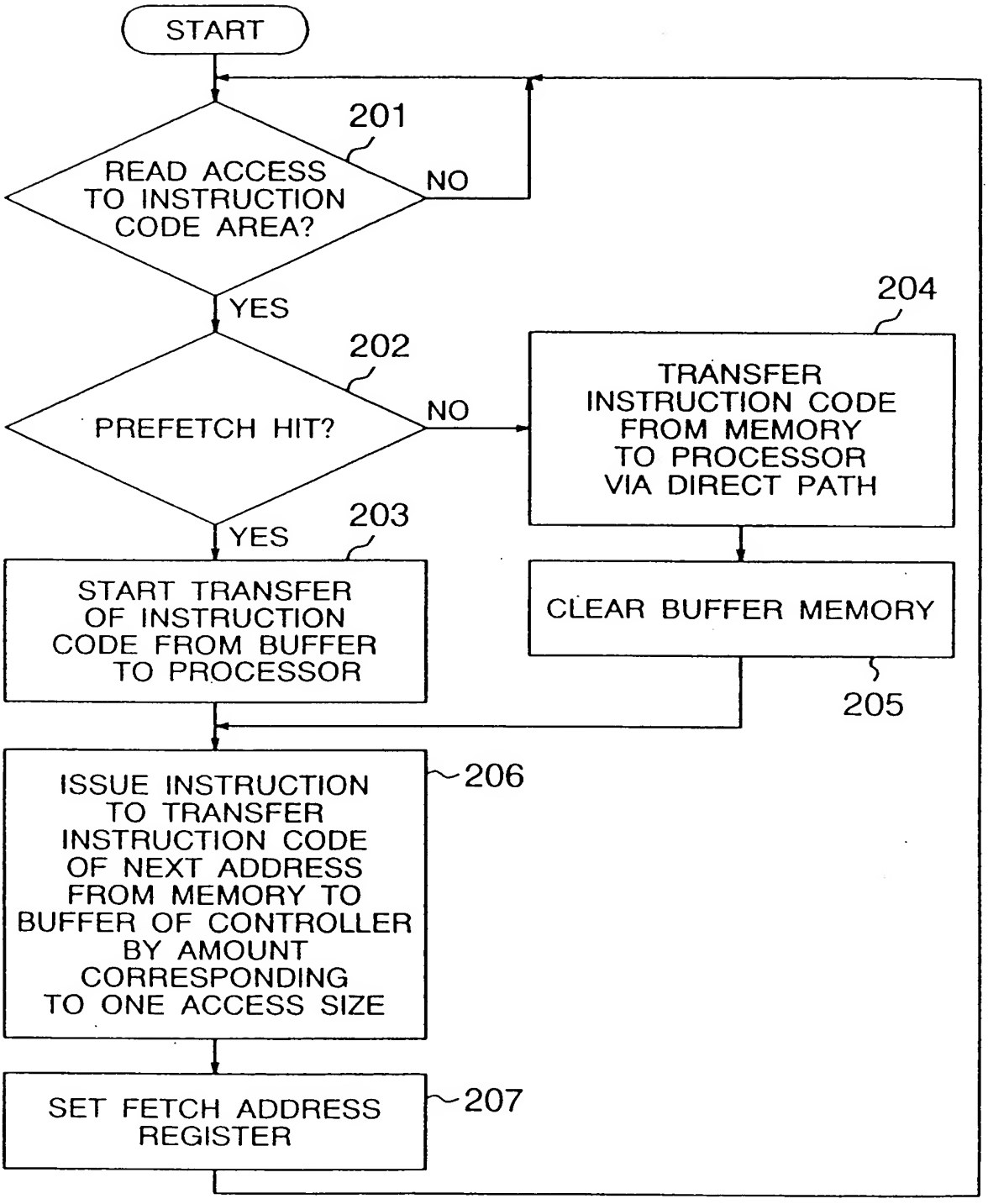
START
201
READ ACCESS TO INSTRUCTION CODE AREA?
NO
YES
202
PREFETCH HIT?
NO
204
TRANSFER INSTRUCTION CODE FROM MEMORY TO PROCESSOR VIA DIRECT PATH
YES
203
START TRANSFER OF INSTRUCTION CODE FROM BUFFER TO PROCESSOR
CLEAR BUFFER MEMORY
205
206
ISSUE INSTRUCTION TO TRANSFER INSTRUCTION CODE OF NEXT ADDRESS FROM MEMORY TO BUFFER OF CONTROLLER BY AMOUNT CORRESPONDING TO ONE ACCESS SIZE
207
SET FETCH ADDRESS REGISTER

FIG. 9

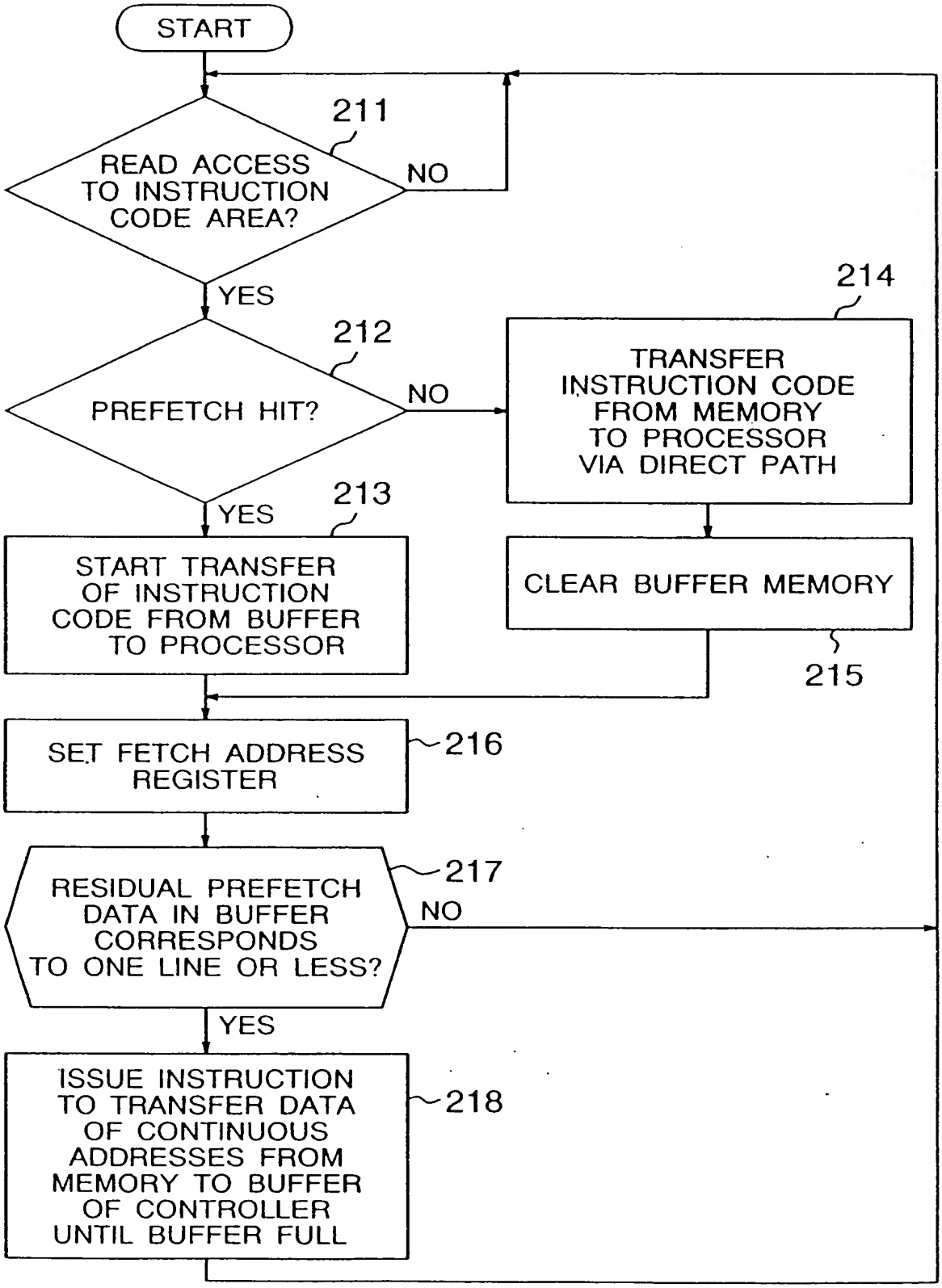
START
211
READ ACCESS TO INSTRUCTION CODE AREA?
NO
YES
212
PREFETCH HIT?
NO
214
TRANSFER INSTRUCTION CODE FROM MEMORY TO PROCESSOR VIA DIRECT PATH
YES
213
START TRANSFER OF INSTRUCTION CODE FROM BUFFER TO PROCESSOR
CLEAR BUFFER MEMORY
215
SET FETCH ADDRESS REGISTER
216
RESIDUAL PREFETCH DATA IN BUFFER CORRESPONDS TO ONE LINE OR LESS?
217
NO
YES
ISSUE INSTRUCTION TO TRANSFER DATA OF CONTINUOUS ADDRESSES FROM MEMORY TO BUFFER OF CONTROLLER UNTIL BUFFER FULL
218

FIG. 10

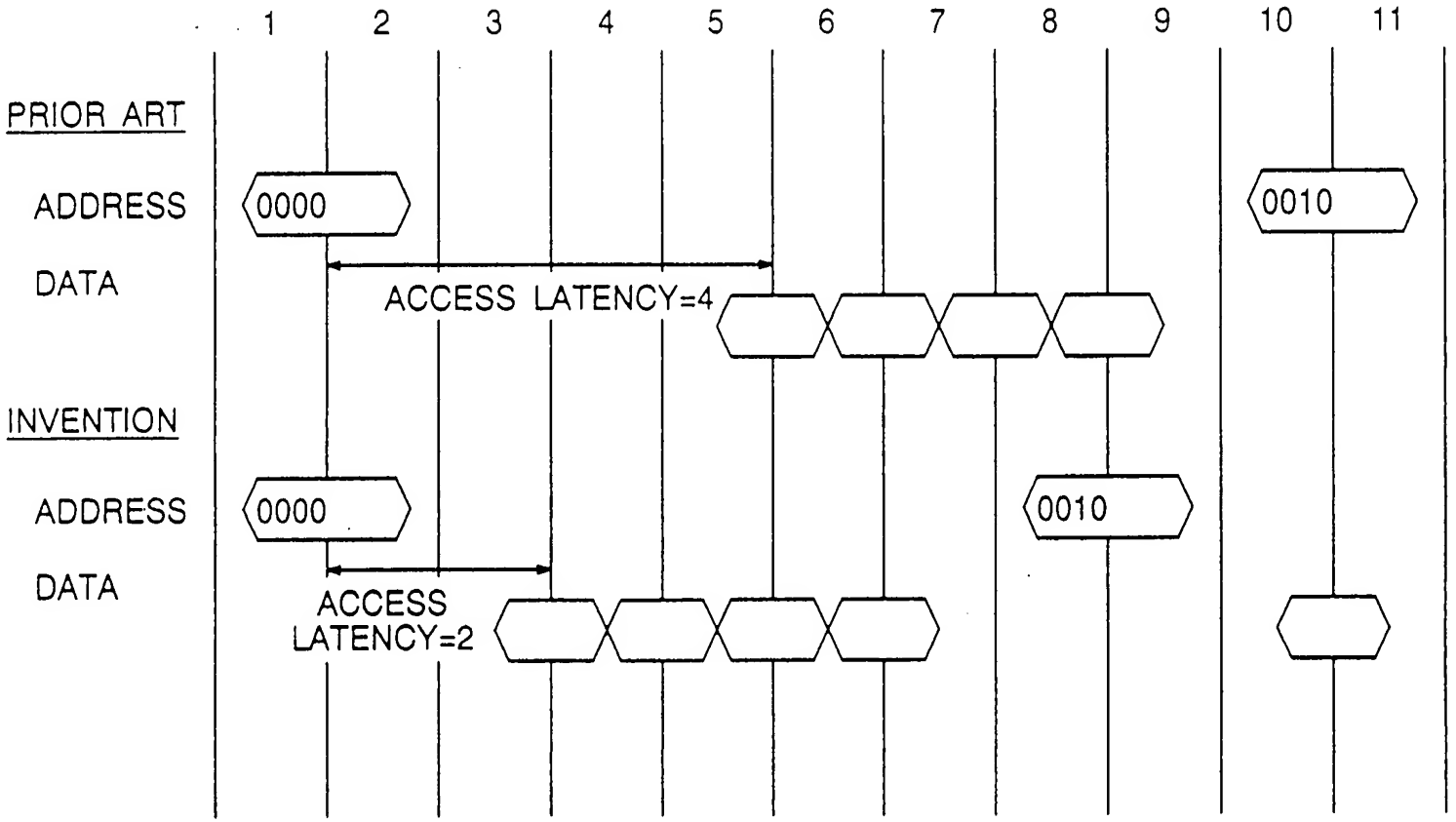
1
2
3
4
5
6
7
8
9
10
11
PRIOR ART
ADDRESS
0000
0010
DATA
ACCESS LATENCY=4
INVENTION
ADDRESS
0000
0010
DATA
ACCESS
LATENCY=2

FIG. 11

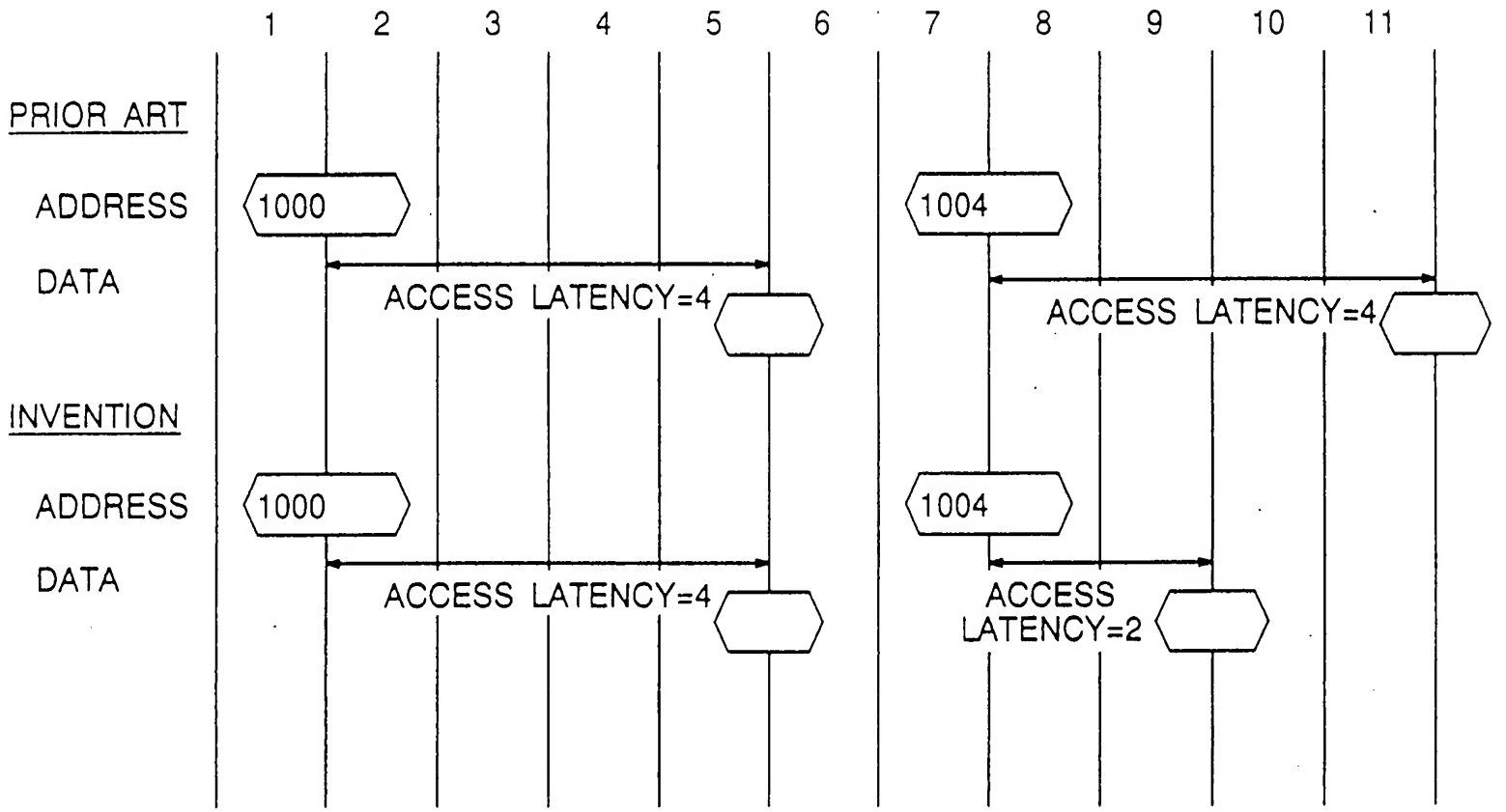
1
2
3
4
5
6
7
8
9
10
11
PRIOR ART
ADDRESS
1000
1004
DATA
ACCESS LATENCY=4
ACCESS LATENCY=4
INVENTION
ADDRESS
1000
1004
DATA
ACCESS LATENCY=4
ACCESS LATENCY=2

FIG. 12

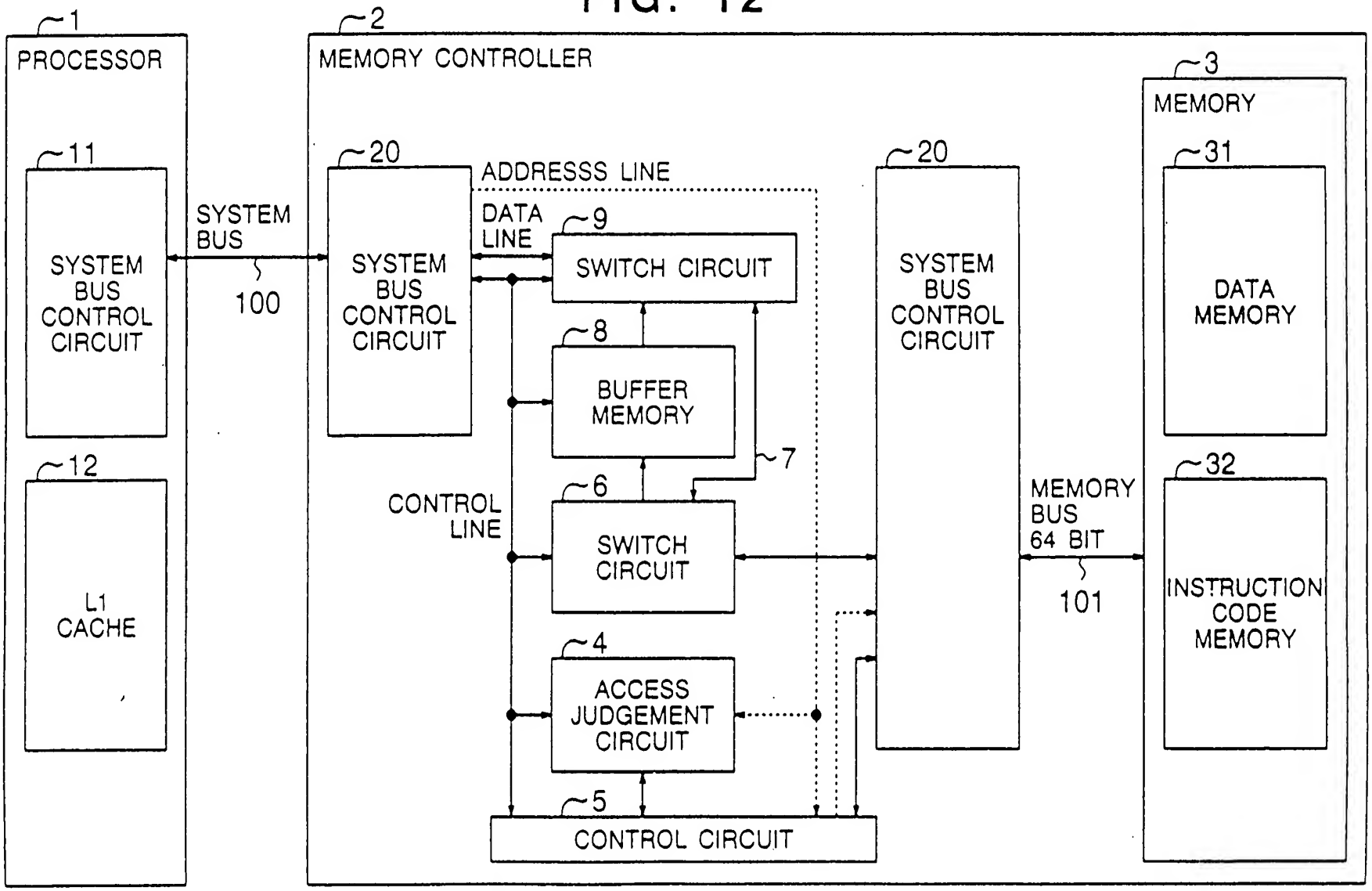
1
PROCESSOR
11
SYSTEM BUS CONTROL CIRCUIT
12
L1 CACHE
SYSTEM BUS
100
2
MEMORY CONTROLLER
20
SYSTEM BUS CONTROL CIRCUIT
ADDRESSS LINE
DATA LINE
9
SWITCH CIRCUIT
8
BUFFER MEMORY
7
CONTROL LINE
6
SWITCH CIRCUIT
4
ACCESS JUDGEMENT CIRCUIT
5
CONTROL CIRCUIT
20
SYSTEM BUS CONTROL CIRCUIT
MEMORY BUS 64 BIT
101
3
MEMORY
31
DATA MEMORY
32
INSTRUCTION CODE MEMORY

FIG. 13